a source region[;] and a drain region, each including a first impurity;

a channel forming region being formed between the source region and the drain region; and

an impurity region [being added with] including [an] a second impurity having an opposite conductive type to the first impurity [said source region and said drain region] and being formed under [said] the channel forming region,

wherein a concentration of the second impurity in the channel forming region is from 1/100 to 1/10 of that in [said] the impurity region, [and]

wherein the second impurity is introduced from a direction of the < 110 > axis with respect to the single semiconductor substrate,

wherein the concentration of the second impurity in the impurity region is in a range of 1 x 10^{18} to 1 x 10^{19} atoms/cm^3,

wherein the concentration of the second impurity in the channel forming region is in a range of 1 x 10^{16} to 1 x 10^{17} atoms/cm^3.

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3. (Amended) A device according to claim 1, [wherein the concentration of the impurity in the impurity region is in a range of 1 x 10^{18} to 1 x 10^{19} atoms/cm^3, and]

wherein the impurity region is substantially not in contact with the source region and the drain region.

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15. (Amended) A device according to claim 1, wherein [said] the semiconductor device is an integrated circuit (IC).

B4 18. (Amended) A device according to claim 1, wherein [said] the semiconductor device is a microprocessor.

B5 21. (Amended) A device according to claim 18, wherein [said] the microprocessor is at least one selected from the group consisting of a RISC processor and an ASIC processor.

24. (Amended) A device according to claim 1, wherein [said] the semiconductor device is at

B6 least one selected from the group consisting of a cellular phone, a personal handy phone system, and a portable computer.

Sub D2 B7 27. (Amended) A device according to claim 1, wherein the impurity region is formed at a depth in a range of [from] 20 to 150 nm from a surface of the single semiconductor substrate.

Sub C2 Please add new claims 29-55.

B8 -- 29. A semiconductor device comprising a plurality of MOSFETs formed in a single semiconductor substrate,

each of the plurality of MOSFETs comprising:

a source region and a drain region each including a first impurity;

a channel forming region being formed between the source region and the drain region;

an impurity region including a second impurity having an opposite conductive type to the first impurity and being formed under the channel forming region;

a pair of LDD regions, wherein one of the pair of LDD regions is formed between the source region and the channel forming region while the other of the pair of LDD regions is formed between the channel forming region and the drain region,

wherein a concentration of the second impurity in the channel forming region is from 1/100 to 1/10 of that in the impurity region,

wherein the second impurity is introduced from a direction of the < 110 > axis with respect to the single semiconductor substrate,

wherein the concentration of the second impurity in the impurity region is in a range of 1 x 10^{18} to 1 x 10^{19} atoms/cm^3,

wherein the second concentration of the impurity in the channel forming region is in a range of 1 x 10^{16} to 1 x 10^{17} atoms/cm^3.--

-- 30. A device according to claim 29, wherein the semiconductor device is an integrated circuit (IC).--

-- 31. A device according to claim 29, wherein the semiconductor device is a microprocessor.--

-- 32. A device according to claim 31, wherein the microprocessor is at least one selected from the group consisting of a RISC processor and an ASIC processor.--

-- 33. A device according to claim 29, wherein the semiconductor device is at least one selected from the group consisting of a cellular phone, a personal handy phone system, and a portable computer.--

-- 34. A device according to claim 29, wherein the impurity region is formed at a depth in a range of 20 to 150 nm from a surface of the single semiconductor substrate.--

-- 35. A semiconductor device comprising a plurality of MOSFETs formed in a single semiconductor substrate,

each of the plurality of MOSFETs comprising:

a source region and a drain region each including a first impurity;

a channel forming region being formed between the source region and the drain region;

an impurity region including a second impurity having an opposite conductive type to the first impurity,

wherein a concentration of the second impurity in the impurity region is in a range of 1×10^{18} to 1×10^{19} atoms/cm^3,

wherein a concentration of the second impurity in the channel forming region is in a range of 1×10^{16} to 1×10^{17} atoms/cm^3,

wherein the impurity region is formed under the source region and the channel forming region while the impurity region is not formed under the drain region.--

-- 36. A device according to claim 35, wherein the semiconductor device is an integrated circuit (IC).--

-- 37. A device according to claim 35, wherein the semiconductor device is a microprocessor.-

-- 38. A device according to claim 37, wherein the microprocessor is at least one selected from the group consisting of a RISC processor and an ASIC processor.--

-- 39. A device according to claim 35, wherein the semiconductor device is at least one selected from the group consisting of a cellular phone, a personal handy phone system, and a portable computer.--

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-- 40. A device according to claim 35, wherein the impurity region is formed at a depth in a range of 20 to 150 nm from a surface of the single semiconductor substrate.--

--41. A device according to claim 35,

wherein the second impurity is introduced from a direction of the < 110 > axis with respect to the single semiconductor substrate.--

Subt C3

-- 42. A semiconductor device comprising at least a CMOS circuit including an n-channel MOSFET and a p-channel MOSFET each being formed in a single semiconductor substrate,

said n-channel MOSFET comprising:

a first source region and a first drain region each comprising a first n-type impurity;

a first channel forming region being formed between the first source region and the first drain region;

a first impurity region including a first p-type impurity and being formed under the first channel forming region;

said p-channel MOSFET comprising:

a second source region and a second drain region each comprising a second p-type impurity;

a second channel forming region being formed between the second source region and the second drain region;

a second impurity region including a second n-type impurity and being formed under the second channel forming region,

wherein a concentration of the first p-type impurity in the first impurity region is in a range of 1×10^{18} to 1×10^{19} atoms/cm^3,

wherein a concentration of the first p-type impurity in the first channel forming region is in a range of 1×10^{16} to 1×10^{17} atoms/cm^3

wherein a concentration of the second n-type impurity in the second impurity region is in a range of 1×10^{18} to 1×10^{19} atoms/cm^3,

wherein a concentration of the second n-type impurity in the second channel forming region is in a range of 1×10^{16} to 1×10^{17} atoms/cm^3.--

-- 43. A device according to claim 42,

wherein the first n-type impurity is arsenic,

wherein the second n-type impurity is phosphorus,

wherein each of the first and second p-type impurity is boron.--

-- 44. A device according to claim 42, wherein the semiconductor device is an integrated circuit (IC).--

-- 45. A device according to claim 42, wherein the semiconductor device is a microprocessor.--

-- 46. A device according to claim 45, wherein the microprocessor is at least one selected from the group consisting of a RISC processor and an ASIC processor.--

-- 47. A device according to claim 42, wherein the semiconductor device is at least one selected from the group consisting of a cellular phone, a personal handy phone system, and a portable computer.--

-- 48. A device according to claim 42, wherein each of the first and second impurity regions is formed at a depth in a range of 20 to 150 nm from a surface of the single semiconductor substrate.--

--49. A device according to claim 42,

wherein each of the first p-type and the second n-type impurities is introduced from a direction of the < 110 > axis with respect to the single semiconductor substrate.--

-- 50. A semiconductor device comprising a plurality of MOSFETs formed in a single semiconductor substrate,

each of the plurality of MOSFETs comprising:

a source region and a drain region each including a first impurity;

a channel forming region being formed between the source region and the drain region;

an impurity region including a second impurity having an opposite conductive type to the first impurity,

wherein a concentration of the second impurity in the channel forming region is from 1/100 to 1/10 of that in the impurity region,

wherein a concentration of the second impurity in the impurity region is in a range of 1×10^{18} to 1×10^{19} atoms/cm^3,

wherein a concentration of the second impurity in the channel forming region is in a range of 1×10^{16} to 1×10^{17} atoms/cm^3,

wherein the impurity region is formed under the source region and the channel forming region while the impurity region is not formed under the drain region.--

-- 51. A device according to claim 50, wherein the semiconductor device is an integrated circuit (IC).--

-- 52. A device according to claim 50, wherein the semiconductor device is a microprocessor.--

-- 53. A device according to claim 52, wherein the microprocessor is at least one selected from the group consisting of a RISC processor and an ASIC processor.--

-- 54. A device according to claim 50, wherein the semiconductor device is at least one selected from the group consisting of a cellular phone, a personal handy phone system, and a portable computer.--

B8 cont

-- 55. A device according to claim 50, wherein the impurity region is formed at a depth in a range of 20 to 150 nm from a surface of the single semiconductor substrate.--

REMARKS

On February 14, 2000, the Examiner issued a Final Rejection in the parent application. On May 12, 2000, Applicants filed a response. On May24, 2000, the Examiner issued an Advisory Action stating that the Applicants' arguments had been considered but were not found to be persuasive. On August 7, 2000, Applicants filed a Notice of Appeal with the appropriate Petition to Extend Time. Applicants are now filing this Preliminary Amendment and CPA application to address the Examiner's prior rejection.

In the Final Rejection, the Examiner is maintaining the rejection of Claims 1-4, 14-15, 18, 21, 24, 27 and 28 under 35 U.S.C. 103(a) as being unpatentable over Chang et al. This rejection is respectfully traversed.

The present invention, as recited in independent amended Claim 1, is directed to a semiconductor device including source and drain regions including a first impurity, a channel forming region and an impurity region which is formed under the channel forming region and includes a second impurity, wherein the second impurity has an opposite conductive type to the first impurity and has a concentration in the channel forming region of 1/100 to 1/10 compared with that in the impurity region, wherein the second impurity is introduced into the impurity region in a direction of